AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A shielded multi-conductor interconnect bus comprising:

a substrate;

a first dielectric layer overlying and supported by at least a portion of said substrate;

a plurality of parallel electrically conductive lines formed on said first dielectric layer, wherein there is no intervening electrically conductive layer between said plurality of parallel electrically conductive lines and said substrate;

a plurality of parallel electrically conductive walls formed on said first dielectric layer, each said electrically conductive wall including an upper section extending vertically above the level of said electrically conductive lines; and

an electrically conductive shield formed in a spaced relation above said electrically conductive lines and in contact with said upper sections of said electrically conductive walls;

wherein said electrically conductive lines and said electrically conductive walls are arranged in pattern wherein one of said electrically conductive walls is located between sets of said electrically conductive lines, each said set of electrically conductive lines including at least one of said electrically conductive lines.

2. The interconnect bus of Claim 1 wherein said first dielectric layer is formed on an upper surface of said substrate, and wherein said first dielectric layer includes a plurality of parallel channels formed therein, each said channel extending vertically down into said first dielectric layer to expose the upper surface of said substrate along at least a portion of said channel, each said electrically conductive wall including a lower section formed in one of said channels.

3. The interconnect bus of Claim 2 wherein said substrate is comprised of silicon and said first dielectric layer comprises a dielectric stack deposited on the upper surface of said substrate, said dielectric stack comprising a lower layer of thermal oxide and an upper layer of silicon nitride.

4. The interconnect bus of Claim 1 further comprising:

a second dielectric layer overlying said electrically conductive lines and said first

dielectric layer, said second dielectric layer having a plurality of channels formed therein permitting said upper sections of said electrically conductive walls to extend vertically upward therethrough to contact said electrically conductive shield.

5. The interconnect bus of Claim 4 wherein said second dielectric layer comprises one of silicon dioxide and silicate glass.

6. The interconnect bus of Claim 2 wherein said electrically conductive lines and said lower sections of said electrically conductive walls are formed from a first layer of doped polysilicon.

7. The interconnect bus of Claim 6 wherein said upper sections of said electrically conductive walls and said electrically conductive shield are formed from a second layer of doped polysilicon.

8. The interconnect bus of Claim 7 wherein said second layer of doped polysilicon comprises two separately deposited layers of doped polysilicon.

9. (Withdrawn)

10. The interconnect bus of Claim 1 wherein each said set of electrically conductive lines includes two of said electrically conductive lines.

11. The interconnect bus of Claim 1 wherein said electrically conductive walls are laterally spaced from each other by no more than 50 microns.

12. The interconnect bus of Claim 1 wherein said electrically conductive walls are laterally spaced from each other by no more than 10 microns.

13. The interconnect bus of Claim 1 further comprising:

at least one electrically conductive line oriented transversely to said parallel electrically

conductive lines and connected to at least one of said parallel electrically conductive lines, said transversely oriented electrically conductive line extending outward from a side of said interconnect bus through a break formed in an outer one of said electrically conductive walls.

14. The interconnect bus of Claim 13 wherein said transversely oriented electrically conductive line is shielded by a pair of electrically conductive walls and an electrically conductive shield supported in a spaced relation above said transversely oriented electrically conductive line.

15. The interconnect bus of Claim 14 wherein said electrically conductive walls and electrically conductive shield shielding said transversely oriented electrically conductive line are respectively joined to said outer one of said electrically conductive walls and said shield overlying said parallel electrically conductive lines.

16-23. (Withdrawn)

24. (Currently Amended) A shielded multi-conductor interconnect bus comprising:

a substrate;

a plurality of electrically conductive lines formed on said substrate, each said electrically conductive line being surrounded by dielectric material along a lengthwise extent of each said electrically conductive line, wherein there are no intervening electrically conductive structures formed between each said electrically conductive line and said substrate;

an electrically conductive shield overlying and spaced above said electrically conductive lines; and

a plurality of electrically conductive walls formed on said substrate, each said electrically conductive wall being in contact along a lower section thereof with said substrate and along an upper section thereof with said electrically conductive shield;

said electrically conductive lines and said electrically conductive walls being arranged in pattern wherein one of said electrically conductive walls is located between sets of said electrically conductive lines, each said set of electrically conductive lines including at least one of said electrically conductive lines.

25. The interconnect bus of Claim 24 wherein said dielectric material surrounding each said electrically conductive line comprises a lower dielectric stack layer and an upper sacrificial layer.

26. The interconnect bus of Claim 25 wherein said upper sacrificial layer is comprised of one of silicon dioxide and silicate glass.

27. The interconnect bus of Claim 25 wherein said substrate is comprised of silicon and said lower dielectric stack layer comprises a lower layer of thermal oxide and an upper layer of silicon nitride.

28. The interconnect bus of Claim 24 wherein said electrically conductive lines and said lower sections of said electrically conductive walls are formed from a first layer of doped polysilicon.

29. The interconnect bus of Claim 28 wherein said upper sections of said electrically conductive walls and said electrically conductive shield are formed from a second layer of doped polysilicon.

30. The interconnect bus of Claim 29 wherein said second layer of doped polysilicon comprises lower and upper layers of doped polysilicon.

31. (Withdrawn)

32. The interconnect bus of Claim 24 wherein each said set of electrically conductive lines includes two of said electrically conductive lines.

33. (Currently Amended) A shielded electrically conductive line comprising:
a substrate;
a first dielectric layer overlying and supported by at least a portion of said substrate;

an electrically conductive line formed on said first dielectric layer, wherein there is no intervening electrically conductive layer between said electrically conductive line and said substrate;

a pair of parallel electrically conductive walls formed on said first dielectric layer, each said electrically conductive wall being located on an opposing side of said electrically conductive line and including an upper section extending above the level of said electrically conductive line; and

an electrically conductive shield formed in a spaced relation above said electrically conductive line and in contact with said upper sections of said electrically conductive walls.

34. The shielded electrically conductive line of Claim 33 wherein said first dielectric layer is formed on an upper surface of said substrate, and wherein said first dielectric layer includes a pair of parallel channels formed therein, each said channel extending vertically down into said first dielectric layer to expose the upper surface of said substrate along at least a portion of said channel, each said electrically conductive wall including a lower section formed in one of said channels.

35. The shielded electrically conductive line of Claim 34 wherein said substrate is comprised of silicon and said first dielectric layer comprises a dielectric stack deposited on the upper surface of said substrate, said dielectric stack comprising a lower layer of thermal oxide and an upper layer of silicon nitride.

36. The shielded electrically conductive line of Claim 33 further comprising:

a second dielectric layer overlying said electrically conductive line and said first dielectric layer, said second dielectric layer having a pair of channels formed therein permitting said upper sections of said electrically conductive walls to extend vertically upward therethrough to contact said electrically conductive shield.

37. The shielded electrically conductive line of Claim 36 wherein said second dielectric layer comprises one of silicon dioxide and silicate glass.

38. The shielded electrically conductive line of Claim 34 wherein said electrically conductive line and said lower sections of said electrically conductive walls are formed from a first layer of doped polysilicon.

39. The shielded electrically conductive line of Claim 38 wherein said upper sections of said electrically conductive walls and said electrically conductive shield are formed from a second layer of doped polysilicon.

40. The shielded electrically conductive line of Claim 39 wherein said second layer of doped polysilicon comprises two separately deposited layers of doped polysilicon.

41. The shielded electrically conductive line of Claim 33 wherein said shielded electrically conductive line is connected to at least one electrically conductive line of a shielded interconnect bus.

42. (New) The interconnect bus of Claim 13 wherein said transversely oriented electrically conductive line is perpendicular to said parallel electrically conductive lines.

43. (New) A shielded multi-conductor interconnect bus comprising:

a substrate;

a first dielectric layer overlying and supported by at least a portion of said substrate;

a plurality of parallel electrically conductive lines formed on said first dielectric layer;

a plurality of parallel electrically conductive walls formed on said first dielectric layer, each said electrically conductive wall including an upper section extending vertically above the level of said electrically conductive lines, wherein said parallel electrically conductive lines and said parallel electrically conductive walls are arranged in pattern wherein one of said parallel electrically conductive walls is located between sets of said parallel electrically conductive lines, each said set of parallel electrically conductive lines including at least one of said parallel electrically conductive lines;

an electrically conductive shield formed in a spaced relation above said electrically conductive lines and in contact with said upper sections of said electrically conductive walls; and

at least one electrically conductive line oriented transversely to said parallel electrically conductive lines and connected to at least one of said parallel electrically conductive lines, said transversely oriented electrically conductive line extending outward from a side of said interconnect bus through a break formed in an outer one of said electrically conductive walls.

44. (New) The interconnect bus of Claim 43 wherein said transversely oriented electrically conductive line is shielded by a pair of electrically conductive walls and an electrically conductive shield supported in a spaced relation above said transversely oriented electrically conductive line.

45. (New) The interconnect bus of Claim 44 wherein said electrically conductive walls and electrically conductive shield shielding said transversely oriented electrically conductive line are respectively joined to said outer one of said electrically conductive walls and said shield overlying said parallel electrically conductive lines.

46. (New) The interconnect bus of Claim 43 wherein said transversely oriented electrically conductive line is perpendicular to said parallel electrically conductive lines.